REMARKS

Claims 1-27 are pending and are rejected. Claims 1, 7, 10 and 16 are currently amended. Claims 2 and 11 are canceled without prejudice. Applicants request reconsideration of the claim rejections.

Claim Rejections Under 35 U.S.C. §103

The following obviousness rejections are asserted in the Office Action:

(1) Claims 1-21 and 25-27 are rejected as being unpatentable over U.S. Patent No. 5,935,428 to Yamamoto in view of U.S Patent No. 4,706,219 to Miyata.

(2) Claims 22-24 are rejected as being unpatentable over Yamamoto and Miyata, and further in view of U.S. Patent No. 5,349,448 to Hirai.

With respect to the above rejection (1), Applicants respectfully submit that at the very least, claims 1, 10, 20, 21 and 25-27 are patentable over the combination of Yamamoto an Miyata. Applicants contend that the obviousness rejections are improperly based on mischaracterizations and misinterpretations of the teachings of Yamamoto and Miyata as applied to the claimed inventions. To illustrate this point, the teachings of the cited references will be discussed with reference to the claims as re-written with the corresponding reference numbers of "similar" elements of the cited references according to the Examiner's characterization of the reference teachings as applied to the claims:

Claim 1:

With regard to claim 1, the Examiner contends that Yamamoto discloses in FIG. 1

A *semiconductor memory device* comprising

an integrated circuit (IC) memory chip comprising an integrated memory circuit and a plurality of address pins, wherein the integrated memory circuit comprises;

a memory cell array **(RAM 2, FIG. 1)**;

a data buffer **(element 11, FIG. 2)** *for processing data read from or written to the memory cell array* **(RAM 2)**; and

a data width control circuit **(the controller 16, FIG. 2)** *for selectively controlling a data width of the data buffer element* **(element 11, FIG. 2)** *in response to one or more address bits of an external address signal applied to one or more address pins of the IC memory chip*

The Examiner's reliance on Yamamoto in this regard is unreasonable and clearly undermined by the unambiguous teachings of Yamamoto, for the following reasons.

Yamamoto clearly teaches that the RAM 2 is a 32 bit-width memory that is connected to a 32 bit CPU over a 32 bit bus (see Col. 4, lines 22-27). There is nothing in Yamamoto that teaches or suggests that the RAM 2 can be dynamically controlled to have a variable I/O data width. Moreover, the Examiner has not shown that any of the memory devices 2, 5, 6 in FIG. 1 of Yamato are controlled to have variable I/O width.

There is no teaching in Yamamoto that the *data buffer* **(element 11, FIG. 2)** *processes data read from or written to the memory cell array* **(RAM 2).** Indeed, Yamamoto discloses that the data buffer (11) and controller (16) are part of a gateway (4) that controls communications of data between the CPU (1) and the ROM (5), memory (6) or devices (7, 8), and that the data buffer (11) is controlled by the controller (16) to latch ***data of 32 bits supplied by the CPU (1)*** (see, Col. 4, lines 58-63).

The Examiner has not shown that data written to or read from the RAM 2 is stored in the data buffer (11) of the gateway (4) in FIGs. 1 and 2 of Yamamoto. Moreover, the Examiner has failed to demonstrate that any of the memory devices 2, 5, 6 in FIG. 1 of Yamamoto are controlled to have a variable I/O data width. The Examiner seemingly fails to understand that the data buffer (11) is used for storing 32 bit data output from the CPU (1) which is transmitted

to the various peripheral devices depending on the data widths of the I/O communication busses of the respective devices. In this regard, the teachings of Yamamoto are way off point.

Moreover, the Examiner's reliance on Yamamoto is fundamentally flawed because the Examiner fails to consider the claim language that the claimed *memory cell array, data buffer and data width control circuit* are part of an integrated memory circuit formed on an integrated circuit (IC) memory chip, i.e., the integrated memory circuit comprises the claimed *memory cell array, data buffer and data width control circuit.*

The Examiner dismisses and ignores this claimed feature by saying in the Response to Arguments section that while Yamamoto does not teach these elements on an integrated circuit, Yamamoto essentially teaches these elements separately. This argument fails to consider the claim limitations in the context of claim 1, as a whole, wherein the *data width control circuit selectively controls a data width of the data buffer element in response to one or more address bits of an external address signal applied to one or more address pins of the IC memory chip* on which the memory cell array, data buffer and data width control circuit are all integrally formed.

The Examiner relies on Miyata to cure the deficiencies of Yamamoto. However, the Examiner's reliance on Miyata is not clearly understood and is seemingly based on a clear misapplication of the reference teachings to the claimed inventions. It should be readily clear that neither reference, Yamamoto nor Miyata teaches or suggests *data width control circuit selectively controls a data width of the data buffer element in response to one or more address bits of an external address signal applied to one or more address pins of the IC memory chip.*

Although Miyata discloses an integrated memory chip comprising a plurality of address pins, the Examiner has not explained how Miyata teaches a "variable data length storage memory", where the data width is controlled by a bit of an external address signal. Miyata

discloses a memory device having a structure that can be modified one time during the course of a manufacturing process to select one of a variety of possible word lengths at the time of manufacturing by selection of a code mask to place the output selection means in either a first or second mode (see, Col. 1, lines 35 ~ Col 2, line 28). A mode selector circuit (1) includes a switch that is adapted to be connected to either ground or VCC in accordance with a code mask to place the memory structure in a ***first or second fixed mode*** where the ROM can have a different amount of input address pins and output terminal (see, cols. 5 and 6, and claim 1 on Col. 7, lines 8-32).

In this regard, there is simply nothing in Miyata that teaches a a variable I/O data width memory circuit having a *data width control circuit that selectively controls a data width of the data buffer element in response to one or more address bits of an external address signal applied to one or more address pins of the IC memory chip.*

For at least the above reasons, the combined teachings of Yamamoto and Miyata are legally and factually deficient to support the obviousness rejection of claim 1. Moreover, to the extent that claims 10, 20, 21 and 25-27 recite the same, similar or related subject matter of claim 1, and to the extent that the Examiner fails to provide a separate obviousness analysis for these claims but merely relies on the same rational for rejecting of claim 1, Applicants contend that claims 10, 20, 21 and 25-27 are clearly non-obvious over the combination of Yamamoto and Miyata for at least the same reasons given for claim 1.

Notwithstanding the above, Applicants have amended the claim 1 and 10 for the sole purpose of further clarifying the claimed subject matter and the patentable distinctions over the cited art of record. With regard to claims 1 and 10, the combination of Yamamoto and Miyata does not disclose or suggest, for example,

wherein the data width control circuit comprises:

a decoder for decoding the one or more address bits of external address signal in response to a data access command to generate a first control signal; and

a data buffer controller, responsive to the first control signal, to generate a second control signal for controlling the data width of the data buffer as recited in claim 1 for example.

In the Final Office Action, the Examiner cites Col. 5, line 64 through Col 6, line 7 and Col. 4, lines 56 -57, of Yamamoto as teaching these limitation (in original claim 2). Applicants respectfully disagree.

Yamamoto teaches in Col 5, line 64 ~ Col. 6, line 7 an address decoder (17) that decodes an address output from the CPU (1) and generated a chip select signal to the appropriate peripheral device , e.g., RAM 2. On a fundamental level, this interpretation is essentially irrelevant to the claimed inventions and is clearly inconsistent with the Examiner's previous characterization. The Examiner initially characterizes the *data with control circuit* as being the controller (16), but from this characterization, the Examiner essentially contends that the controller (16) (claimed data width control circuit) comprises the main address decoder (17) (claimed decoder). Clearly, the controller (16) in FIG. 2 does not include the main bus address decoder (17).

Moreover, the Examiner notes that the decoder (17) outputs a chip select signal to the RAM 2, but yet fails to explain how the *data buffer controller* (which the Examiner now characterizes as the controller 16) is *responsive to the first control signal* (i.e., what the Examiner initially characterizes as the the "chip select signal" output from the decoder (17)), *to generate a second control signal for controlling the data width of the data buffer (11).* Clearly, the chip

select signal (supposed "first control signal") output from the decoder (17) (supposed "decoder" of "data width control circuit" for decoding address bits) does not control the controller (16) to control the data width of the data buffer (11).

It is clear that the above obviousness analysis is based on several strained and inconsistent interpretations of the same claim limitations to improperly fit the claims to the reference teachings. However, the Examiner cannot fairly support an obviousness rejection by interpreting the claim language in several different, inconsistent ways to simply fit the claim language to the teachings of the cited references. These inconsistencies in claim interpretations underscore the erroneousness of the obviousness rejections.

Moreover, claim 10 now includes the limitations of claim 11, i.e., *wherein the data width control circuit comprises:*

a decoder which is activated in response to a read command signal or write command signal to decode the one or more address bits of the external address to generate a first control signal;

a data input buffer controller which is activated in response to the write command signal to generate a second control signal for controlling the data width of the data input buffer based on the first control signal; and

a data output buffer controller which is activated in response to the read command signal to generate a second control signal for controlling the data width of the data output buffer based on the first control signal.

In the Office Action, the Examiner does not specifically explain the basis for rejecting claim 11 (now incorporated in claim 10) other than relying on the same reasons given for claim 2 (now incorporated in claim 1). Therefore, it may be said that the above claim features are not disclosed or suggested by the cited references for at least the same reasons given above for claim 1 (incorporating the subject matter of claim 2) .

With regard to the above listed obviousness rejection (2) for claims 22-24 , given that the obviousness rejection is primarily based in part, on the primary references Yamamoto and Miyata as as applied to independent claim 21, it is respectfully submitted that the obviousness rejection of claim 22 and 24 are legally deficient for at least the same reasons given for claim 21. Moreover, the cited reference Hirai clearly does not cure the deficiencies of Yamamoto or Miyata as noted above with regard. Accordingly, the withdrawal of the obviousness rejections is respectfully requested.

Respectfully submitted,

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